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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,190	11/15/2000	Woong-Kwon Kim	3430-0138P	8112

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER
NGUYEN, HOAN C

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,190	KIM, WOONG-KWON	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's arguments with respect to AMENDED claims 1-10 and 15-27 have been considered but are moot in view of the new ground(s) of rejection. The amended independent claims raised the new issue: a color filter overlapping only edge portions of the source and drain electrodes. Therefore, this is a Final Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 6-8, 15-16, 21-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1).

Midorikawa et al. teach a liquid crystal display device (LCD) comprising

- a substrate 11,
- a gate electrode 16 over the substrate;
- a semiconductor layer aligned with a gate electrode. In according to claims 16 and 21, for forming TFT, it is conventional well-known art that the doped semiconductor layer deposited on the pure semiconductor layer to generate the drain and source electrodes;

- the gate insulating layer 12 between the gate electrode and the semiconductor layer;
- a source electrode and a drain electrode electrically connected with the semiconductor layer,
- a color filter layer 24a-c overlapping only edge portions of the source and drain electrodes;
- pixel electrode on the color filter layer without a planarization layer.

Guehler et al. teach a liquid crystal display device (LCD) comprising

- a planarization layer 16 formed on the color filter and the source and drain electrodes; the planarization layer having a opening exposing the drain electrode thereunder for contact hole;
- pixel electrode 12 formed on the planarization layer 16 and electrical contacting the drain electrode via the planarization opening.

2. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1) applied to claims 1 and 6 above, and further view of Kashiwazaki et al. (US6162510A).

Kashiwazaki discloses (Figs. 6C-F) the conventional TFT including:

- forming a first layer/a semiconductor layer 104 on gate insulating layer 1-3;
- forming etch stopper layer 105, the doped semiconductor layer 106 covering the semiconductor layer and the etch stopper layer;

- forming second layer/passivation film 110 over the first layer and the etch stop layer;

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a LCD device as Midorikawa et al. disclosed with the conventional TFT having the etch stop layer for preventing first layer made of semiconductor from being etched.

3. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1) applied to claims 1 and 6 above, and further view of Murade (US6297862B1).

Murade (Figs. 3a-4d) discloses the LCD device comprising light shielding layer 7 formed between the substrate 10 and TFT and an insulating layer 11 covering the light-shielding layer 7.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a LCD device as Midorikawa et al. disclosed with the light shield below TFT for protecting TFT from incident light.

4. Claims 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1) applied to claims 15 and 22 above, and further view of Kashiwazaki et al. (US6162510).

Kashiwazaki discloses (Figs. 6C-F) the TFT including:

- forming a gate electrode 102;

- forming a gate insulating layer 103;
- depositing a semiconductor layer 104 on gate insulating layer;
- patterning the semiconductor layer to form an active layer made of amorphous silicon (claim 25);
- forming etch stopper layer 105, the doped semiconductor layer 106 covering the semiconductor layer and the etch stopper layer;
- forming the source and drain electrodes 107/108 on the doped semiconductor layer with etching a portion of the doped semiconductor layer between the source and drain electrodes to form a channel region;
- etching a portion of the doped semiconductor layer between the source and drain electrodes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a LCD device as Midorikawa et al. disclosed with the conventional TFT having the etch stop layer for preventing first layer made of semiconductor from being etched.

5. Claims 18, 19, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1) applied to claims 15 and 22 above, and further view of Murade (US6297862B1).

With respected to claims 18 and 24, Murade (Figs. 3a-4d) discloses the LCD device comprising light shielding layer 7 formed between the substrate 10 and TFT and an insulating layer 11 covering the light shielding layer 7.

With respected to claim 19, Murade (Figs. 3a-4d) discloses the LCD device, wherein the TFT further includes:

- a poly-silicon active layer 1 having source and drain region at the end portions thereof;
- a gate insulating layer 12 on a central portion of the active layer, the gate electrode 2 being formed on the gate insulating layer;
- an inner layer insulator 13 formed entirely over the substrate, having a first and a second contact hole which respectively expose a portion of source and drain regions 1a/1b therebelow, wherein the source and drain electrodes are formed on the interlayer insulator to respectively contact the source and drain regions.

With respected to claim 20, Murade (Figs. 3a-4d) discloses the LCD device, wherein the active layer 1 is made of poly-silicon for less light sensitive thus the LCD device could be used in presence of a large quantity of light [the other reference of Sato et al. (US6327006B1) also applies to same feature].

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a LCD device as Midorikawa et al. disclosed with (a) the light shield below TFT for protecting TFT, (b) the active layer 1 is

made of poly-silicon for less light sensitive thus the LCD device could be used in presence of a large quantity of light.

6. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Midorikawa et al. (US6281955B1) in view of Guehler et al. (US6221543B1) applied to claims 15 and 22 above, and further view of Ohkubo et al. (US6166786A).

Ohkubo et al. (Figs. 3a-e) disclose the method of manufacturing a LCD, wherein forming the TFT includes:

- forming a semiconductor 10 made of polysilicon film (col. 5, line 35);
- forming a gate insulating layer 15, a with of the gate insulating layer being smaller than that of the semiconductor layer for ion-doped on the semiconductor (col. 39-51);
- forming a gate electrode 16 on the gate insulating layer;
- ion-doped and exposed portion of semiconductor layer to define source and drain regions;
- forming an interlayer insulator 31 (Fig. 12) entirely over the substrate, the interlayer including a source region contact hole to expose a portion electrode therebelow, and a drain region contact hole to expose a portion of the drain electrode therebelow;
- forming source and drain electrodes to be in electrical contact with the source and drain regions.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a LCD device as Guehler et al. disclosed with manufacturing the conventional polysilicon-TFT, wherein (a) forming a gate insulating layer, a with of the gate insulating layer being smaller than that of the semiconductor layer for ion-doped on the semiconductor, (b) a semiconductor 10 made of polysilicon film for low temperature manufacturing.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (703) 306-0472. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SIKES L WILLIAM can be reached on (703) 308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-8178 for regular communications and (703) 308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0530.

HOAN C. NGUYEN
Examiner
Art Unit 2871

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July 11, 2002

TOAN TON
PRIMARY EXAMINER